REMARKS

Claims 33-55 have not been amended, and are still pending in the present application.

Claims 33-55 stand rejected under either 35 USC 102(b) or 35 USC 103(a) as being unpatentable over USP 5,574,475 to Callahan, Jr. et al. ("Callahan"). These rejections are respectfully traversed.

Independent ***claims 33, 39, 46, 51*** each recites a driver circuit for a display that has "a plurality of transistor groups, each transistor group formed by a plurality of serially coupled transistors, each transistor group being coupled to a separate one of the voltage levels and the output". This is illustrated, for example, in FIG. 5 of the present application, where there are four serially coupled transistors coupled between the output and voltage level V0, four serially coupled transistors coupled between the output and voltage level V2, four serially coupled transistors coupled between the output and voltage level V4, and four serially coupled transistors coupled between the output and voltage level V6,

In contrast, Callahan does not teach or suggest a plurality of serially coupled transistors coupled to a separate one of the voltage levels and the output. In particular, in FIGS. 3A, 6 and 7 of Callahan, the divided voltage is provided by a switch circuit (42 in FIG. 3A, 106 in FIG. 6 and 124 in FIG. 7). Each switch circuit 42, 106, 124 has one input connected with a different divided voltage. Furthermore, each switch circuit is made up of a PMOS and an NMOS coupled in parallel. Active regions 128 and 126 in FIG. 7 are combined to act as a NAND gate. The same applies for the circuits 41 in FIG. 3A and the circuit 102 in FIG. 6. Based on the output of the NAND gates, one of the switches will turn on for outputting one of the divided voltages Vref1-Vref8 in FIG. 3A.

Thus, Callahan does not disclose "a plurality of transistor groups, each transistor group formed by a plurality of serially coupled transistors, each transistor group being coupled to a separate one of the voltage levels and the output". Callahan uses a different architecture to output divided voltage by using a NAND gate and a switch. For these reasons, claims 33, 39, 46, 51 (and the claims depending therefrom) are submitted to be in condition for allowance.

In light of the above, all pending claims are submitted to be in condition for allowance. Reconsideration and allowance of this application is respectfully solicited. The Examiner is invited to telephone the undersigned if there are any amendments or issues that can be resolved in a phone conversation.

Respectfully Submitted,

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CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal service as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Date: April 8, 2005 By: _____
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